

CLAIMS

What is claimed is:

- 1 1. A method comprising:
 - 2 interfacing a first device with a second device;
 - 3 clocking at least a portion of the second device with a first clock signal;
 - 4 transmitting a clock signal source from the second device to the first device;
 - 5 transmitting a second clock signal from the first device to the second device, the
 - 6 second clock signal being the clock signal source delayed by a
 - 7 propagation delay;
 - 8 adjusting a phase of the clock signal source such that a phase of the second clock
 - 9 signal is substantially in alignment with a phase of the first clock signal;
 - 10 and
 - 11 transmitting data clocked by the second clock signal from the first device to the
 - 12 second device.
- 1 2. The method of claim 1, wherein the second device is a high speed analog
- 2 semiconductor device.
- 1 3. The method of claim 1, wherein the first device is a CMOS semiconductor device.
- 1 4. The method of claim 1, wherein the phase of the clock signal source is adjusted
- 2 by modifying the frequency of the clock signal source.
- 1 5. The method of claim 1, wherein the data is transmitted from the second device to
- 2 the first device without an initiation sequence.

1 6. The method of claim 1, further comprising receiving a reference clock signal,
2 wherein the first clock signal and the clock signal source are generated from the
3 reference clock signal.

1 7. The method of claim 1, further comprising reducing a frequency of the clock
2 signal source if a frequency of the second clock signal is less than the frequency
3 of the clock signal source.

1 8. A transmitter comprising:
2 a subpart that is clocked by a first clock signal;
3 a first interface connection to a device, the device transmitting data to the
4 transmitter using the first interface connection;
5 a second interface connection to the device, the transmitter transmitting a clock
6 signal source to the device using the second interface connection;
7 a third interface connection to the device, the device transmitting a second clock
8 signal to the transmitter using the third interface connection, the second
9 clock signal being the clock signal source delayed by a propagation delay
10 through a portion of the device; and
11 a phase detection unit, the phase detection unit adjusting the phase of the clock
12 signal source to align the phase of the second clock signal with the phase
13 of the first clock signal.

1 9. The transmitter of claim 8, further comprising a reference clock signal
2 connection, the transmitter receiving a reference clock signal using the reference
3 clock connection.

1 10. The transmitter of claim 9, further comprising a clock multiplier unit, the
2 transmitter using the clock multiplier unit to generate the first clock signal and the
3 clock signal source from the reference clock signal.

1 11. The transmitter of claim 8, wherein the phase detection unit adjusts the phase of
2 the clock signal source by adjusting the frequency of the clock signal source.

1 12. The transmitter of claim 8, wherein the transmitter reduces a frequency of the
2 clock signal source if a frequency of the second clock signal is less than the
3 frequency of the clock signal source.

1 13. The transmitter of claim 8, wherein the phase detection unit is a set-reset latch
2 based phase frequency detector.

1 14. A self-synchronizing interface comprising:
2 a first interface connection between a first device and a second device, the second
3 device transmitting a first clock signal to the first device through the first
4 interface connection;
5 a second connection between the first device and the second device, the first
6 device transmitting a delayed version of the first clock signal to the second
7 device, the second device modifying the phase of the first clock signal
8 such that the phase of the delayed version of the first clock signal aligns
9 with the phase of a second clock signal, at least a portion of the second
10 device being clocked by the second clock signal; and

11 a third interface connection between the first device and the second device, the
12 first device transmitting data to the second device through the third
13 interface connection, the data being clocked by the delayed version of the
14 first clock signal.

1 15. The interface of claim 14, wherein the second device modifies the phase of the
2 first clock signal by modifying the frequency of the first clock signal.

1 16. The interface of claim 14, wherein the second device reduces a frequency of the
2 first clock signal source if a frequency of the delayed version of the first clock
3 signal is less than a frequency of the clock signal source.

1 17. A data communication system comprising;
2 a first subsystem, the first subsystem receiving a first clock signal, the first
3 subsystem further transmitting data that is clocked by a second clock
4 signal, the second clock signal being the first clock signal delayed by a
5 propagation delay through at least a portion of the first subsystem; and
6 a second subsystem, the second subsystem transmitting the first clock signal to
7 the first subsystem and receiving the data and the second clock signal from
8 the first subsystem, at least a portion of the second subsystem being
9 clocked by a third clock signal, the second subsystem modifying the phase
10 of the first clock signal to align the phase of the second clock signal with
11 the phase of the third clock signal.

1 18. The data communications system of claim 17, wherein the first subsystem
2 includes a buffer memory.

1 19. The data communications system of claim 17, wherein the second subsystem
2 operates at a higher speed than the first subsystem.

1 20. The data communications system of claim 17, wherein the second subsystem
2 modifies the phase of the first clock signal by modifying the frequency of the first
3 clock signal.

1 21. The data communications system of claim 17, wherein the second subsystem
2 reduces the frequency of the first clock signal if the frequency of the second clock
3 signal is below the frequency of the first clock signal.

1 22. The data communications system of claim 17, wherein the second subsystem
2 includes a phase frequency detector.

1 23. The data communications system of claim 22, wherein the phase frequency
2 detector is a set-reset latch based phase frequency detector.

1 24. A method comprising:
2 interfacing a first device with a second device;
3 generating a first clock signal and a second clock signal;
4 clocking at least a portion of the second device with the first clock signal;
5 transmitting the second clock signal from the second device to the first device;
6 generating a third clock signal, the third clock signal being the second clock
7 signal after propagating through a portion of the first device;
8 transmitting the third clock signal and data clocked by the third clock signal from
9 the first device to the second device;

10 detecting phases and frequencies of the first clock signal and the third clock signal
11 and comparing the phase of the first clock signal to the phase of the third
12 clock signal; and
13 if the phase of the first clock signal and the phase of the third clock signal are not
14 in alignment, modifying the phase of the second clock signal until the
15 phase of the third clock signal is aligned with the phase of the first clock
16 signal.

- 1 25. The method of claim 24, further comprising reducing a frequency of the second
2 clock signal if the frequency of the third clock signal is below the frequency of
3 the second clock signal.
- 1 26. The method of claim 25, wherein the frequency of the third clock signal is below
2 the frequency of the second clock signal because the frequency of the second
3 clock signal is above a maximum frequency that can be generated by the first
4 device.